Marked Up Claims

1.(Amended) A circuit for monitoring the voltage spikes occurring in a power converter system containing a bus having a resistive parameter [R] (R) and an inductive [parameters] parameter [L] (L) comprising:

a first comparator circuit having first and second inputs;

a first reference level voltage source connected to [a] the first [one] input of the first comparator circuit first and second inputs for providing a first voltage level input signal;

a second comparator circuit having first and second inputs;

a second reference level voltage source connected to [a first] the second input [one] of the second comparator circuit first and second inputs to provide a second voltage level input signal;

a time constant circuit

the second [ones] input of the first comparator circuit first and second inputs and the first input of the second comparator circuit first and second inputs being connected in common through the time constant circuit to the bus of the power converter circuit and responsive to a voltage spike [V_{spike}] (V_{spike}) thereon;

wherein the first comparator circuit produces an output signal when a voltage spike on the bus exceeds the voltage level of the first voltage level input signal, and wherein the second comparator circuit produces an output signal when a voltage spike on the bus is lower than the voltage level of the second voltage level input signal.

2.(Amended) The circuit of claim 1 wherein the power converter system bus includes a sensing resistor [R_{sense}] (R_{sense}), and a capacitor [C_{sense}] (C_{sense}) to block dc signal components and to provide a [R/C] (RC) time constant selected so that the voltage value measured across the sensing resistor [R_{sense}] (R_{sense}) is the value of the voltage spike [V_{spike}] (V_{spike}).

4.(Amended) The circuit of claim 1 wherein the power converter system further includes an inverter portion having a current [i_{inv}] (i_{inv}) and wherein a voltage [V_L] (V_L) of the inductive parameter [L] (L) of the bus is approximately equal to [V_{spike}] (V_{spike}) which is equal to (L)(di_{inv}/dt).

5.(Amended) A method for monitoring the voltage spikes [V_{spike}] (V_{spike}) occurring in a power converter system containing a bus having a resistive parameter [R] (R) and an inductive parameter [L] (L) comprising the steps of:

C. obtaining a voltage [V_L] (VL) of the inductive parameter [L] (L) of the bus that is approximately equal to [V_{spike}] (V_{spike}), which is equal to (L)(di_{inv}/dt);

D. providing a first reference level voltage signal;

C. providing a second reference level voltage signal;

E. blocking the dc components of the bus voltage and providing a [sense] sensing resistor [Rsense] (Rsense) in the bus of the power converter system;

E. comparing the voltage across the [sense] sensing resistor [Rsense] (Rsense) with the first reference level signal to provide a first comparison signal when the voltage across the [sense] sensing resistor is greater than the first reference level signal; and

F. comparing the voltage across the [sense] sensing resistor [Rsense] (Rsense) with the second reference level signal to provide a second comparison signal when the voltage across the [sense] sensing resistor is lower than the second reference signal.

6.(Amended) The method of claim 5 wherein [the power converter system bus further includes] the step of blocking the dc signal components of the bus further includes [with] using a sensing capacitor [Csense] (Csense) [and] to provide a [R/C] (RC) time constant selected so that the voltage value across the sensing resistor [Rsense] (Rsense) is the value of the voltage spike [Vspike] (Vspike).

7.(Amended) The method of claim [1] 5 further including the step of combining the first and second comparison signals to provide a fault indicating signal.

8.(Amended) The method of claim [1] 5 further including the step of providing a power converter system including an inverter portion having a current [iinv] (iinv) and wherein a

voltage [V_L] (VL) of the inductive parameter [L] (L) of the bus is approximately equal to [V_{spike}] (Vspike) which is equal to (L) (di_{inv}/dt) where [i_{inv}] (i_{inv}) is the inverter current.

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